Application No.: 10/728,262
Reply to Office Action of February 23, 2005

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (original) A method for regenerating clock signals, comprising:

converting clock signals having either single- ended clock pulses or differential clock pulses into clock signals having substantially the same voltage swing.

2. (original) The method recited in claim 1 wherein the single-ended clock pulses are provided by a TTL logic circuit and wherein the differential clock pulses are produced by an ECL logic circuit.

3. (original) A method for regenerating clock signals, comprising:

providing a source of clock signals, such source producing either single- ended clock pulses or differential clock pulses, such clock signals being fed to a regeneration circuit, such regeneration circuit converting such clock signals having either the single- ended clock pulses or the differential clock pulses into clock signals having substantially the same voltage swing.

4. (currently amended) A clock regeneration circuit, comprising:

a differential amplifier having a non-inverting input terminal and an inverting input terminal;

a first voltage divider network coupled between a pair of reference voltages and the non-inverting input terminal;

a second voltage divider network coupled between the pair of reference voltages and the inverting input terminal;

wherein the first and second voltage divider networks produce the same differential voltage swing for both single-ended or differential clock source signals voltage at the inverting and non-inverting input terminals.

5. (original) The clock regeneration circuit recited in claim 4 wherein the first voltage divider network includes a pair of resistors, a first one of the pair of resistors, R1, being connected between a first one of the pair of reference voltages and the non-inverting input and a second one of the pair of resisters, R2, being connected between the non-inverting input and the second one of the pair of reference voltages.

6. (original) The clock regeneration circuit recited in claim 5 wherein the second voltage divider network includes a pair of resistors, a first one of the pair of resistors, R3, being connected between a first one of the pair of reference voltages and the inverting input and a second one of the pair of resisters, R4, being connected between the inverting input and the second one of the pair of reference voltages.

7. (original) The clock regeneration circuit recited in claim 6 wherein R1 is has the same resistance as R3 and R2 has the same resistance as resistor R4.

8. (currently amended) ~~The clock regeneration circuit recited in claim 7~~ A clock regeneration circuit, comprising:

a differential amplifier having a non-inverting input terminal and an inverting input terminal;

a first voltage divider network coupled between a pair of reference voltages and the non-inverting input terminal;

a second voltage divider network coupled between the pair of reference voltages and the inverting input terminal;

wherein the first and second voltage divider networks produce the same voltage at the inverting and non-inverting input terminals

including a transmission line coupled between a source of clock signals and the input terminals, and wherein such transmission line has a characteristic impedance Zo, and wherein R1*R2/(R1+R2) equals Zo.

9. (original) The clock regeneration circuit recited in claim 8 wherein the source of clock

pulses is an emitter coupled logic circuit and wherein the potential difference provided by the pair of reference voltages voltage, Vcc, times (R2/(R1+R2)) and Vcc, times (R3/(R3+R4)) are selected to provide predetermined proper terminating voltages to the emitter coupled logic circuit.

10. (currently amended) The clock regeneration circuit recited in claim 8 wherein the source of clock pulses is a transistor-transistor logic circuit having an output transistor, such output transistor having an emitter and collector coupled between the pair of reference potentials, and including a coupling resistor R5 serially connected between the collector electrode and the non-inverting input though the transmission line, such resistor R5 being selected to provide a predetermined proper voltage swing across the non-inverting and inverting inputs.

11. (original) A method for regenerating clock signals, comprising:

providing a source of clock signals, such source having either TTL logic circuit for producing single- ended lock pulses or ECL logic circuit for producing differential clock pulses,

providing a clock pulse regeneration circuit;

feeding to clock signals to the regeneration circuit, such regeneration circuit converting such clock signals having either the single-ended clock pulses or the differential clock pulses into clock signals having substantially the same voltage swing;

providing such regeneration circuit with:

a differential amplifier having a non-inverting input terminal and an inverting input terminal;

a first voltage divider network coupled between a pair of reference voltages and the non-inverting input terminal;

a second voltage divider network coupled between the pair of reference voltages and the inverting input terminal;

wherein the first and second voltage divider networks produce the same voltage at the inverting and non-inverting input terminals.

12. (original) The method recited in claim 11 wherein the regeneration circuit the first voltage divider network is provided with a pair of resistors, a first one of the pair of resistors,

R1, being connected between a first one of the pair of reference voltages and the non-inverting input and a second one of the pair of resisters, R2, being connected between the non-inverting input and the second one of the pair of reference voltages.

13. (original) The method recited in claim 12 wherein the second voltage divider network is provided with a pair of resistors, a first one of the pair of resistors, R3, being connected between a first one of the pair of reference voltages and the inverting input and a second one of the pair of resisters, R4, being connected between the inverting input and the second one of the pair of reference voltages.

14. (original) The method recited in claim 13 wherein R1 is has the same resistance as R3 and R2 has the same resistance as resistor R4.

15. (original) The method recited in claim 14 including providing a transmission line coupled between a source of clock signals and the input terminals, and wherein such transmission line has a characteristic impedance Zo, and wherein R1*R2/(R1+R2) equals Zo.

16. (original) The method recited in claim 15 including connecting to the transmission line either:

an emitter coupled logic circuit for producing the clock pulses and wherein the potential difference provided by the pair of reference voltages voltage, Vcc, times (R2/(R1+R2)) and Vcc, times (R3/(R3+R4)) are selected to provide predetermined proper terminating voltages to the emitter coupled logic circuit; or

an transistor-transistor logic circuit for producing the clock pulses having an output transistor, such output transistor having an emitter and collector coupled between the pair of reference potentials, and including a coupling resistor R5 serially connected between the collector electrode and the non-inverting input though the transmission line, such resistor R5 being selected to provide a predetermined proper voltage swing across the non-inverting and inverting inputs

17 (New) The clock regeneration circuit recited in claim 8 wherein the first voltage divider

network includes a pair of resistors, a first one of the pair of resistors, R1, being connected between a first one of the pair of reference voltages and the non-inverting input and a second one of the pair of resisters, R2, being connected between the non-inverting input and the second one of the pair of reference voltages.

18. (New) The clock regeneration circuit recited in claim 17 wherein the second voltage divider network includes a pair of resistors, a first one of the pair of resistors, R3, being connected between a first one of the pair of reference voltages and the inverting input and a second one of the pair of resisters, R4, being connected between the inverting input and the second one of the pair of reference voltages.

19. (New) The clock regeneration circuit recited in claim 18 wherein R1 is has the same resistance as R3 and R2 has the same resistance as resistor R4.

20. (New) The clock regeneration circuit recited in claim 19 a resistor serially connected between a source of clock pulses and one of the input terminals of the differential amplifier;